

**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently Amended) A plasma display panel, comprising:

a first substrate;

a second substrate facing the first substrate with a discharge space therebetween;

a sealing layer located between the first substrate and the second substrate,

wherein the sealing layer has a thermal expansion coefficient of approximately  $65 \times 10^{-7} \sim 80 \times 10^{-7}/^{\circ}\text{C}$ ;

at least one of a buffer layer or a dielectric layer formed between the first substrate and the sealing layer, wherein the at least one of the buffer layer or the dielectric layer has the following composition: PbO at a ratio of 45% to 55%, B<sub>2</sub>O<sub>3</sub> at a ratio of 10% to 20% and SiO<sub>2</sub> at a ratio of 15%-25%; and

a protective film formed on the at least one of the buffer layer or the dielectric layer, wherein the at least one of the buffer layer or the dielectric layer has a thermal expansion coefficient different from the thermal expansion coefficient of the sealing layer.

2. (Canceled)

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3. (Currently Amended) The plasma display panel according to claim 1, wherein the buffer layer has ~~[[a]]~~the thermal expansion coefficient different from a thermal expansion coefficient of the first substrate.

4-6. (Canceled)

7. (Previously Presented) The plasma display panel according to claim 1, wherein the first substrate has a thermal expansion coefficient of approximately  $80 \times 10^{-7} \sim 95 \times 10^{-7} / ^\circ\text{C}$ .

8. (Canceled)

9. (Currently Amended) The plasma display panel according to claim 1, wherein the buffer layer has ~~[[a]]~~the thermal expansion coefficient of approximately  $72 \times 10^{-7} \sim 86 \times 10^{-7} / ^\circ\text{C}$ .

10. (Canceled)

11. (Previously Presented) The plasma display panel according to claim 1, wherein the plasma display panel includes both the buffer layer and the dielectric layer such that the buffer layer is provided between the first substrate and the dielectric layer and such that the dielectric layer is provided between the buffer layer and the protective film.

12. (Previously Presented) The plasma display panel according to claim 11, wherein the buffer layer is formed to extend from the dielectric layer.

13. (Previously Presented) The plasma display panel according to claim 11, wherein the buffer layer is separately formed of a different material than the dielectric layer.

14-25. (Canceled)

26. (Currently Amended) A plasma display panel, comprising:

a first substrate;

a second substrate arranged with respect to the first substrate such that a discharge space is provided therebetween;

a sealing layer between the first substrate and the second substrate, wherein the sealing layer has a thermal expansion coefficient of approximately  $65 \times 10^{-7} \sim 80 \times 10^{-7} / ^\circ\text{C}$ ; and

at least one of a buffer layer or a dielectric layer formed between the first substrate and the sealing layer, wherein the at least one of the buffer layer or the dielectric layer has a thermal expansion coefficient of approximately  $72 \times 10^{-7} / ^\circ\text{C}$  to  $85 \times 10^{-7} / ^\circ\text{C}$ , and wherein the thermal expansion coefficient of the at least one of the buffer layer or the dielectric layer is different from the thermal expansion coefficient of the sealing layer.

27. (Previously Presented) The plasma display according to claim 26, wherein the sealing layer extends in a longitudinal direction from a first end to a second end, the first end located proximal to the first substrate and the second end located proximal to the second substrate, the buffer layer provided only in the area between the first end of the sealing layer and the first substrate.

28. (Previously Presented) The plasma display according to claim 26, further comprising:

another sealing layer between the first substrate and the second substrate; and

another buffer layer formed between the first substrate and the another sealing layer, the another buffer layer to compensate thermal stress of the first substrate and the another sealing layer.

29. (Previously Presented) The plasma display panel according to claim 28, wherein the at least one of the buffer layer or the dielectric layer is the buffer layer, and the plasma display panel further comprises:

an upper dielectric layer formed on the first substrate between the buffer layer and the another buffer layer; and

a protective film formed on the upper dielectric layer.

30. (Previously Presented) The plasma display panel according to claim 26, wherein the thermal expansion coefficient of the buffer layer is different from a thermal expansion coefficient of the first substrate.

31-38. (Canceled)

39. (Previously Presented) The plasma display panel according to claim 26, wherein the at least one of the buffer layer or the dielectric layer has the following composition: PbO at a ratio of 45% to 55%, B<sub>2</sub>O<sub>3</sub> at a ratio of 10% to 20% and SiO<sub>2</sub> at a ratio of 15% to 25%.

40. (Previously Presented) The plasma display panel according to claim 1, further comprising electrodes formed on the first substrate.

41. (Previously Presented) The plasma display panel according to claim 26, further comprising electrodes formed on the first and second substrates.

42-43. (Canceled)

44. (Previously Presented) The plasma display panel according to claim 1, wherein the at least one of the buffer layer of the dielectric layer has a thickness greater than 35  $\mu\text{m}$  and less than 39  $\mu\text{m}$  between the sealing layer and the first substrate.

45. (Previously Presented) The plasma display panel according to claim 26, wherein the at least one of the buffer layer of the dielectric layer has a thickness greater than 35  $\mu\text{m}$  and less than 39  $\mu\text{m}$  between the sealing layer and the first substrate.